WHAT IS CLAIMED IS:

1. A reframer, comprising:

a first circuit that detects a frame start point of input data based on a frame alignment signal defined in a framed data of a digital hierarchy signal; and

a second circuit that excludes the input data having an improper start point based on a frame start point detecting value, and that outputs reframed data having a normal frame format.

2. The reframer of claim 1, wherein the first circuit includes:

an input selecting circuit that shifts the input data, maps respective bits of the shifted input data, and selects a plurality of checking patterns on a bit by bit basis according to the shifted input data;

a frame start point detecting circuit that receives the checking patterns outputted from the input selecting circuit, and that detects the frame start point which designates a start location of the frame alignment signal as a frame start point detecting value;

an initial value setting circuit that sets an initial value for counting improper input data based on the frame start point detecting value, and that generates a control signal; and

a counter that counts a number of input data bits having improper data, as count results, from the frame start point, according to the control signal and the initial value.

3. The reframer of claim 2, wherein the input selecting circuit includes:

a first shifter that shifts the input data into a first format and that sequentially outputs the first format shifted input data in parallel to the second circuit.

4. The reframer of claim 3, wherein the input selecting circuit further includes:

a second shifter that also receives the input data having the digital hierarchy structure, shifts the input data into a second format different from the first format according to a designated clock signal, and outputs the second format shifted input data in parallel;

a bit grouping circuit that maps the second format shifted input data to form the plurality of checking patterns according to a designated rule, and outputs groups of the checking patterns; and

a checking pattern selecting output circuit that selectively outputs the plurality of checking patterns outputted from the bit grouping circuit at successive checking periods.

5. The reframer of claim 2, wherein the input selecting circuit maps portions of the shifted input data from an upper bit, and forms a plurality of checking patterns, each checking pattern having the same length as the frame alignment signal.

6. The reframer of claim 5, wherein the input selecting circuit sets a last portion of the shifted input data from a first period, as a first data portion for a next period, and sequentially maps the shifted framed data.

7. The reframer of claim 2, wherein the frame start point detecting circuit repeatedly performs a start point detecting operation until a predetermined frame alignment signal is detected, and determines the frame start point detecting value according to an input data bit order, to indicate a frame alignment signal start bit.

8. The reframer of claim 7, wherein the frame start point detecting value is continuously maintained until a reset signal is inputted or a power source is turned off.

9. The reframer of claim 2, wherein the second circuit includes a frame alignment circuit that aligns the shifted input data according to the frame start point detecting value and the count result, and that outputs the aligned shifted input data as reframed data.

10. The reframer of claim 9, wherein the frame alignment circuit locates a frame start bit among the shifted input data based on the frame start point detecting value, and

excludes data bits having an improper start point among the shifted input data according to the count result.

11. An apparatus for checking a loss of frame, comprising;

a first circuit that detects a frame alignment signal in a framed data of a digital hierarchy signal; and

a second circuit that checks whether the framed data is normal, and provides a releasing state according to a checking result.

12. The apparatus of claim 11, wherein the first circuit includes:

a detector that checks first constant bits inputted on a frame start pulse location of the framed data, and generates one of a releasing enable signal or a declaring enable signal based on the first constant bits.

13. The apparatus of claim 12, wherein the second circuit includes a release circuit that, according to the releasing enable signal, counts the number of the first constant bits as the frame count result of a releasing state, and outputs a releasing signal when the first constant bits of the reframed data are the same as the first constant bits of the frame alignment signal, and are continuously inputted over the predetermined number of frames.

14. The apparatus of claim 13, wherein the releasing signal maintains a first releasing value when the first constant bits are inputted abnormally over the predetermined number of frames on the frame start pulse location of the framed data; and

the releasing signal maintains a second frame releasing value when the first constant bits are inputted normally over the predetermined number of frames.

15. The apparatus of claim 12, wherein the second circuit includes a declaration circuit that, according to the declaring enable signal, counts a number of the first constant bits as a frame count result of a declaring state, and outputs a declaring signal when the first constant bits of the reframed data are different than the first constant bits of the frame alignment signal and are continuously inputted over a predetermined number of frames.

16. The apparatus of claim 15, wherein the second circuit further includes a release circuit that, according to the releasing enable signal, counts the number of the first constant bits as the frame count result of a releasing state, and outputs a releasing signal when the first constant bits of the reframed data are the same as the first constant bits of the frame alignment signal, and are continuously inputted over the predetermined number of frames.

17. The apparatus of claim 16, further comprising:

a determination circuit that receives the declaring signal and the releasing signal from the declaration circuit and the release circuit, respectively, and outputs a state signal that indicates a last state of the framed data.

18. The apparatus of claim 16, wherein the declaration circuit includes:

a sub-frame counter that measures a sub-frame length of a circuit frame according to a designated clock signal;

a frame start pulse generator that counts a number of the sub-frames based on the sub-frame length, and provides a frame start pulse signal to the detector at every frame based on the sub-frame length and the number of sub-frames;

a first counter that receives the framed data, the frame count result of the releasing state and the releasing signal from the release circuit, the declaring enable signal from the detector, the sub-frame length and the number of sub-frames, and checks whether the frame count result of the releasing state is continuously inputted over the predetermined number of frames on the frame start pulse location of the framed data; and

a first output circuit that generates and outputs the declaring signal according to the frame count result of the declaring state.

19. The apparatus of claim 16, wherein the release circuit includes:

a second counter circuit that receives the reframed data, the releasing enable signal from the detector, the frame count result of the declaring state, and the declaring signal from the declaration circuit, and checks whether the frame count result of the declaring state is continuously inputted over the predetermined number of frames on the frame start pulse location of the framed data, and

a second output circuit for outputting a releasing signal according to the count result of the releasing state.

20. The apparatus of claim 15, wherein the declaring signal maintains a first declaring value when the first constant bits are inputted abnormally over the predetermined number of frames on the frame start pulse location of the framed data; and

the declaring signal maintains a second declaring value when the first constant bits are inputted normally over the predetermined number of frames.

21. The apparatus of claim 11, further comprising a third circuit that outputs a state indication signal.

22. An integrated circuit for a digital communication, comprising:

a reframer, including:

a first circuit that detects a frame start point of input data based on a frame alignment signal defined in a framed data of a digital hierarchy signal, and

a second circuit that excludes the input data having an improper start point based on a framed start point detecting value, and that outputs reframed data having the frame alignment signal; and

a loss of frame checking apparatus coupled to the reframer, wherein the loss of frame checking apparatus includes:

a third circuit that detects the frame alignment signal in the reframed data, and

a fourth circuit that checks whether the reframed data has a normal frame format, and provides a releasing state according to the checking result.

23. The integrated circuit of claim 22, wherein

the third circuit includes a detector that checks first constant bits inputted on a frame start pulse location of the framed data, and generates one of a releasing enable signal or a declaring enable signal based on the first constant bits; and

the fourth circuit includes:

a declaration circuit that, according to the declaring enable signal, counts a number of the first constant bits as a frame count result of a declaring state, and outputs a declaring signal when the first constant bits of the reframed data are different than when first constant buts of the frame alignment signal, and are continuously inputted continuously over constant frames;

a release circuit that, according to the releasing enable signal, counts the number of the first constant bits as the frame count result of a releasing state, and outputs a releasing signal when the first constant bits of reframed data are the same as the first constant bits of the frame alignment signal, and are continuously inputted over the predetermined number of frames.

a determination circuit that receives the declaring signal and the releasing signal from the declaration circuit and the release circuit, respectively, and outputs a state signal that indicates a last state of the framed data.

24. The integrated circuit of claim 22, further comprising:

a serial to parallel converter that converts serial data to parallel data;

an input selector that selectively transfers one of the parallel data and an input channel data as the input data;

a parallel to serial converter that converts the reframed data into parallel formats a serial data; and

an output selector that selectively outputs one of the converted serial data and the reframed data.

25. The integrated circuit of claim 22, wherein the first circuit includes:

an input selecting circuit that shifts the input data, maps respective bits of the shifted input data, and selects a plurality of checking patterns on a bit by bit basis according to the shifted input data;

a frame start point detecting circuit that receives the checking patterns outputted from the input selecting circuit, and that detects the frame start point which designates a start location of the frame alignment signal as a frame start point detecting value;

an initial value setting circuit that sets an initial value for counting improper input data based on the frame start point detecting value, and that generates a control signal; and

a counter that counts a number of input data bits having improper data, as count results, from the frame start point, according to the control signal and the initial value.

26. The integrated circuit of claim 25, wherein the input selecting circuit includes:

a first shifter that shifts the input data into a first format and that sequentially outputs the first format shifted input data in parallel to the second circuit;

a second shifter that also receives the input data having the digital hierarchy structure, shifts the input data into a second format different from the first format according to a designated clock signal, and outputs the second format shifted input data in parallel;

a bit grouping circuit that maps the second format shifted input data to form the plurality of checking patterns according to a designated rule, and outputs groups of the checking patterns; and

a checking pattern selecting output circuit that selectively outputs the plurality of checking patterns outputted from the bit grouping circuit at successive checking periods.

27. The integrated circuit of claim 25, wherein the input selecting circuit maps portions of the shifted input data from an upper bit, and forms a plurality of checking patterns, each checking pattern having the same length as the frame alignment signal.

28. The integrated circuit of claim 25, wherein the frame start point detecting circuit repeatedly performs a start point detecting operation until a

predetermined frame alignment signal is detected, and determines the frame start point detecting value according to an input data bit order, to indicate a frame alignment signal start bit.

29. The integrated circuit of claim 25, wherein the second circuit includes a frame alignment circuit that aligns the shifted input data according to the frame start point detecting value and the count result, and that outputs the aligned shifted input data as reframed data.

30. An integrated circuit for digital communication, comprising a plurality of reframers on a signal chip, wherein each reframer comprises:

a first circuit that detects a frame start point of input data based on a frame alignment signal defined in a framed data of a digital hierarchy signal; and

a second circuit that excludes the input data having an improper start point based on a frame start point detecting value, and that outputs reframed data having a normal frame format.

31. The integrated circuit of claim 30, wherein each first circuit includes:

an input selecting circuit that shifts the input data, maps respective bits of the shifted input data, and selects a plurality of checking patterns on a bit by bit basis according to the shifted input data;

a frame start point detecting circuit that receives the checking patterns outputted from the input selecting circuit, and that detects the frame start point which designates a start location of the frame alignment signal as a frame start point detecting value;

an initial value setting circuit that sets an initial value for counting improper input data based on the frame start point detecting value, and that generates a control signal; and

a counter that counts a number of input data bits having improper data, as count results, from the frame start point, according to the control signal and the initial value.